control the output overlay provides additional advantages since the video data can be subject to graininess and noise.

Certificate of Correction Change: Column 14, line 3, delete "an" and insert therefor --can--.

Column 14, lines 1-5 have been reproduced as follows:

Although the present invention and its advantages have been described in detail, it should be understood that various changes, substitutions and alterations can be made herein without departing from the spirit and scope of the invention as defined by the appended claims.

IN THE UNMODIFIED CLAIMS:

Submitted herewith are the following claim amendments which formally incorporate changes from a Certificate of Correction issued in U.S. Patent 5,598,525. No bracketing or underline is required since these changes were already part of the issued patent by virtue of a Certificate of Correction. To facilitate printing, the entire claim, as changed by the Certificate of Correction, has been reproduced.

2. (Amended) The controller of claim 1 and further comprising output selection circuitry for selecting for output between graphics data received from said first pipeline and data received from said second pipeline, said selection circuitry operable to:

in a first mode, pass data from said first pipeline; and

in a second mode, pass data from said second pipeline when said data corresponds to a selected display position of a display window.

5. (Amended) The controller of claim 1 wherein said circuitry for retrieving maintains a stream of graphics data to said first pipeline and provides video data to said second pipeline when a display raster scan reaches a display position of a window.

7. (Amended) The controller of claim 1 wherein said second pipeline includes a first first-in-first-out memory for receiving data for a first display line of pixels in memory and a second first-in-first-out memory for receiving data from a second display line of pixels in memory.

8. (Amended) The controller of claim 7 wherein said first display line is adjacent in memory to said second display line.

9. (Amended) The controller of claim 7 further comprising output selection circuitry wherein said output selection circuitry comprises:

an output selector for selecting between data from said second pipeline and data from said first pipeline in response to a selection control signal;

a register for maintaining a plurality of overlay control bits;

window position control circuitry for selectively generating a position control signal when a word of said data stream from said second pipeline falls within a display window;

color comparison circuitry for comparing words of said data stream from said first pipeline with a color key and for providing in response a color comparison control signal; and

a control selector for selectively providing said selection control signal in response to said overlay control bits in said register and at least one of said position control and color comparison control signals.

14. (Amended) The controller of claim 13 wherein said output selector circuitry is further operable to select between graphics data output from a color look-up table and true color data output from said graphics pipeline.

19. (Amended) The circuitry of claim 18 wherein said output selector circuitry further includes a third control input coupled to certain bits of said graphics pipeline, said

output selector circuitry further operable to select between data on said respective video and graphics pipelines in response to said certain bits presented to said selector circuitry.

20. (Amended) The circuitry of claim 18 wherein said window position control circuitry comprises:

a window x-position counter operable to count from a loaded x-position value in response to a video clock, said x-position counter reloading in response to a display horizontal synchronization signal;

a window y-position counter operable to count from a loaded y-position value in response to said horizontal synchronization signal, said y-position counter reloading in response to a display vertical synchronization signal;

CRT position circuitry operable to maintain counts corresponding to a current display pixel; and

comparison circuitry operable to compare current counts in said window counters with said current counts held in said CRT position circuitry and generate in response said first control signal.

23. (Amended) The circuitry of claim 13 wherein said video pipeline comprises:

a first-in/first-out memory for receiving a first stream of words of data from said frame buffer;

a second first-in/first-out memory disposed in parallel with said first first-in/first-out memory for receiving a second stream of words of data from said frame buffer; and

interpolation circuitry for selectively generating an additional word of data by interpolating a word of said first stream and a word of said second stream data output from said first and second first-in/first-out memories.

24. (Amended) The controller of claim 13 wherein said first port comprises a dual-aperture port.

25. (Amended) A display system comprising:

a first backend pipeline for processing data;

a second backend pipeline for processing graphics data disposed in parallel to said first processing pipeline;

a multi-format frame buffer memory having on-screen and off-screen areas each operable to allow said frame buffer to simultaneously store data in graphics and video formats;

an input port for receiving both graphics and video data, each word of said data associated with an address directing said word to be processed as either graphics or video data;

circuitry for writing a word of said playback data into a selected one of said areas of said multi-format memory;

memory control circuitry for controlling the transfer of data between said first backend pipeline and said frame buffer and between said second backend pipeline and said frame buffer;

a display unit; and

overlay control circuitry for selecting for output to said display unit between data provided by said first backend pipeline and data provided by said second backend pipeline.

26. (Amended) The display system of claim 25 wherein said second backend pipeline includes:

a first first-in-first-out memory for receiving first selected data;

a second first-in-first-out memory disposed in parallel to said first first-in-first-out memory for receiving second selected data; and

interpolation data for generating additional data by interpolating data output from said respective first and second first-in-first-out memories.

28. (Amended) The display system of claim 25 further comprising a video front-end pipeline for inputting video data into a selected one of on-screen and off-screen spaces of said frame buffer comprising:

a video data port for receiving video data from a real time data source; and

input control circuitry for receiving framing signals associated with said real time data and generating corresponding addresses to said selected one of said spaces in response.

29. (Amended) The display system of claim 28 wherein said video front-end pipeline further comprises encoding circuitry for packing said video data prior to storage in said selected one of said spaces.

30. (Amended) The display system of claim 28 wherein said video front-end pipeline further comprises multiplexing circuitry for selecting between video data received through said video data port and data received from a dual aperture port.

35. (Amended) The system of claim 34 further comprising selection control circuitry for generating an output control signal for controlling said output selector comprising:

a control selector having a plurality of data inputs coupled to a register, said register for storing a plurality of overlay control bits; and

color comparison circuitry operable to compare bits of data output from said graphics pipeline with a color key and provide in response a control signal to a control input of said control selector.

36. (Amended) The system of claim 34 further comprising window position control circuitry operable to provide a second control signal to a second control input of said control selector when data from said video pipeline falls within a display window.

39. (Amended) The controller of claim 38 further comprising output selection circuitry for selecting for output between graphics data received from said first pipeline and video data received from said second pipeline.

44. (Amended) The display controller of claim 43 wherein said circuitry for selectively retrieving is operable to retrieve at least one said word of video data from said